IN THE CLAIMS

Please amend Claims 1 – 15 as follows:

1. (Previously Presented) A data carrier for the storage of data,

which data carrier has a first interface for communication with a first communication device and

which data carrier has a second interface for communication with a second communication device and

which data carrier includes an electrical circuit arrangement,

which circuit arrangement includes a first voltage supply means, a first clock generator, and a first signal conversion means of the first interface and a second voltage supply means, a second clock generator, and a second signal conversion means of the second interface and

which circuit arrangement has memory means for the storage of data, which memory means has a first storage location, a second storage location, and a third storage location, and which circuit arrangement has a first memory access means, arranged between the first interface and the memory means, for accessing the first storage location, the third storage location, and not the second storage location of the memory means and which circuit arrangement has a second memory access means, arranged between the second interface and the memory means, for accessing the second storage location, the third storage location, and not the first storage location of the memory means and

which circuit arrangement has access enabling means which enable the first storage location to be accessed only by the first memory access means, characterized

in that the data carrier has additional memory access means adapted to cooperate with the second memory access means and adapted to access the first storage location and designed to verify an access authorization for the access to the first storage location, and

in that after a positive result of the verification of the access authorization the second memory access means can, in addition, access the first storage location via the additional memory access means and via the first memory access means.

2. (Previously Presented) A data carrier as claimed in Claim 1, characterized in that the additional memory access means are included in the first memory access means.

3. (Previously Presented) A data carrier as claimed in Claim 1, characterized in that the additional memory access means include access code verification means for the verification of an access code, and

in that a first access code from the second memory access means as well as a second access code can be applied to the access code verification means, which second access code can be calculated from data stored in the first storage location, and in that agreement of the first access code and the second access code is prerequisite for the positive result of the verification of the access authorization.

4. (Previously Presented) A data carrier as claimed in Claim 3, characterized in that an access code calculation means has been provided for the calculation of the calculable second access code, and

in that the access code calculation means is adapted to execute a triple DES encryption process.

5. (Previously Presented) A data carrier as claimed in Claim 3, characterized

in that the additional memory access means have, in addition to the access code verification means, access condition verification means for the verification of an access condition, and

in that a first access condition from the second memory access means as well as a second access condition can be applied to the access condition verification means, which second access condition can be determined from data stored in the first storage location, and

in that agreement of the first access code and the second access code as well as agreement of the first access condition and the second access condition are prerequisite for the positive result of the verification of the access authorization.

6. (Previously Presented) A data carrier as claimed in Claim 1, characterized

in that the electrical circuit arrangement of the data carrier takes the form of an integrated circuit.

7. (Previously Presented) An electrical circuit arrangement for a data carrier for the storage of data,

which circuit arrangement includes a first voltage supply means, a first clock generator, and a first signal conversion means of the first interface for communication with a first communication device and

which circuit arrangement includes a second voltage supply means, a second clock generator, and a second signal conversion means of a second interface for communication with a second communication device and

which circuit arrangement has memory means for the storage of data, which memory means has a first storage location, a second storage location, and a third storage location, and which circuit arrangement has a first memory access means, arranged between the first voltage supply means, the first clock generator, and the first signal conversion means of the first interface and the memory means, for accessing the first storage location, the third storage location, and not the second storage location of the memory means and

which circuit arrangement has a second memory access means, arranged between the second voltage supply means, the second clock generator, and the second signal conversion means of the second interface and the memory means, for accessing the second storage location, the third storage location, and not the first storage location of the memory means and

which circuit arrangement has access enabling means which enable the first storage location to be accessed only by the first memory access means, characterized

in that the circuit arrangement has additional memory access means adapted to cooperate with the second memory access means and adapted to access the first storage location and designed to verify an access authorization for the access to the first storage location, and

in that after a positive result of the verification of the access authorization the second memory access means can, in addition, access the first storage location via the additional memory access means and via the first memory access means.

8. (Previously Presented) A circuit arrangement as claimed in Claim 7, characterized in that the additional memory access means are included in the first memory access means.

9. (Previously Presented) A circuit arrangement as claimed in Claim 7, characterized

in that the additional memory access means include access code verification means for the verification of an access code, and

in that a first access code from the second memory access means as well as a second access code can be applied to the access code verification means, which second access code can be calculated from data stored in the first storage location, and

in that agreement of the first access code and the second access code as well as agreement of the first access condition and the second access is prerequisite for the positive result of the verification of the access authorization.

10. (Previously Presented) A circuit arrangement as claimed in Claim 9, characterized in that an access code calculation means has been provided for the calculation of the calculable second access code, and

in that the access code calculation means is adapted to execute a triple DES encryption process.

11. (Previously Presented) A circuit arrangement as claimed in Claim 9, characterized

in that the additional memory access means have, in addition to the access code verification means, access condition verification means for the verification of an access condition, and

in that a first access condition from the second memory access means as well as a second access condition can be applied to the access condition verification means, which second access condition can be determined from data stored in the first storage location, and

in that agreement of the first access code and the second access code as well as agreement of the first access condition and the second access condition are prerequisite for the positive result of the verification of the access authorization.

12. (Previously Presented) A circuit arrangement as claimed in Claim 7, characterized in that the electrical circuit arrangement takes the form of an integrated circuit.

13. (Currently Amended) A method of accessing a memory means of a data carrier having a first storage location and a second storage location, the method comprising:

storing data in at least the first storage location of the memory means,

enabling the first storage location to be accessed directly only by ~~the~~ a first memory access means,

applying access authorizations for access to the first storage location to additional memory access means,

verifying the applied access authorizations with the aid of the additional memory access means, and

accessing, after verification of the access authorizations and in the case of a positive result of the verification, the first storage location indirectly by a second memory access means via the additional memory access means and via the first memory access means.

14. (Previously Presented) A method as claimed in Claim 13, characterized in that during the verification of the access authorizations a first access code is compared with a second access code by means of access code verification means, and

in that the first access code is applied from the second memory access means, and the second access code is calculated from data stored in the first storage location, and

in that agreement of the first access code and the second access code is prerequisite for the positive result of the verification.

15. (Previously Presented) A method as claimed in Claim 14, characterized in that during the verification of the access authorizations, in addition to the comparison of the

first access code and the second access code with the aid of the access code verification means, a first access condition is compared with a second access condition with the aid of access condition verification means, and

in that the first access condition is applied from the second memory access means to the access condition verification means and the second access condition is determined from data stored in the first storage location, and

in that agreement of the first access code and the second access code as well as agreement of the first access condition and the second access condition are prerequisite for the positive result of the verification.